19-4803; Rev 0; 4/01

MAXIM

10.7Gbps EAM Driver

General Description

The MAX3935 is designed to drive an electro-absorption modulator (EAM) at data rates up to 10.7Gbps. It provides programmable output levels through externally adjustable bias and modulation currents. This EAM driver is fabricated with Maxim's in-house second-generation SiGe process.

The MAX3935 accepts differential ECL or ground-referenced CML clock and data-input signals. Inputs are terminated with on-chip 50Ω resistors. An input-data retiming latch can be used to reject input-pattern-dependent jitter if a clock signal is available.

The driver can modulate EAM devices at amplitudes up to 3.0Vp-p when the device impedance is 50Ω. Typical (20% to 80%) edge speeds are 34ps. The output has an on-chip 75Ω resistor for back termination. The MAX3935 allows for an EAM bias voltage up to 1.2V.

The MAX3935 also includes an adjustable pulse-width control circuit to precompensate for asymmetrical EAM characteristics.

Applications

SONET OC-192 and SDH STM-64 Transmission Systems

DWDM

Metro and Long Haul Transmitters

Add/Drop Multiplexer

Features

- ♦ **Single -5.2V Power Supply**
- ♦ **Low 110mA Supply Current**
- ♦ **34ps Typical Rise/Fall-Time**
- ♦ **Up to 10.7Gbps (NRZ) Operation**
- ♦ **On-Chip Termination Resistors**
- ♦ **Programmable Modulation Voltage Up to 3.0Vp-p**
- ♦ **Programmable EAM Bias Voltage Up to 1.2V**
- ♦ **Adjustable Pulse-Width Control**
- ♦ **Selectable Data Retiming Latch**
- ♦ **Modulation Enable Control**
- ♦ **ESD Protection**

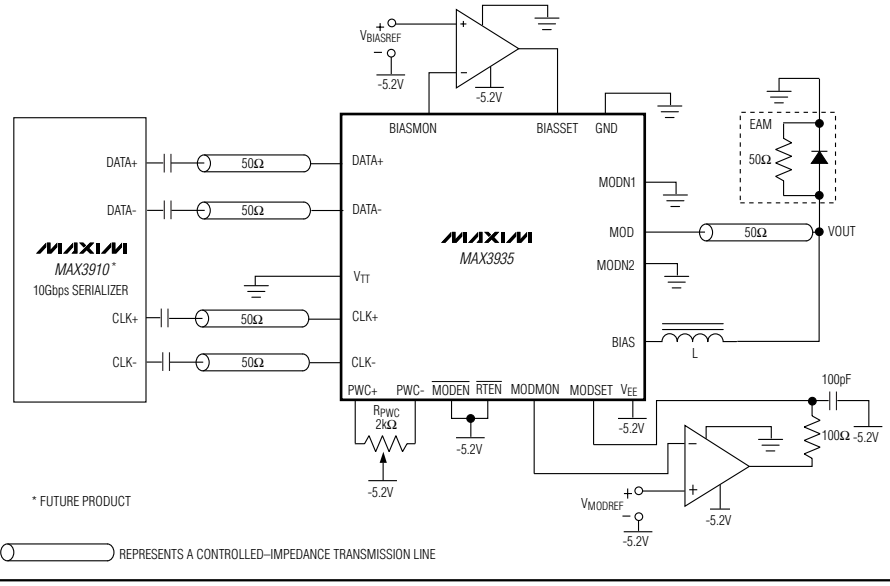
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3935EGJ	-40°C to +85°C	32 QFN-EP*

**Exposed pad*

Pin Configuration appears at end of data sheet

Typical Application Circuit



†Covered by U.S. patent number 5,883,910.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{EE} .....-6.0V to +0.5V
V_{TT}.....(V_{EE} - 0.5V) to +0.5V
DATA+, DATA- and CLK+, CLK- .....(V_{TT} - 1.2V) to the lower of (V_{TT} + 1.2V) or +0.5V
$\overline{MODEN}$, $\overline{RTEN}$, PWC+, and PWC- .....(V_{EE} - 0.5V) to +0.5V
MODSET and BIASSET Voltage .....(V_{EE} - 0.5V) to (V_{EE} + 1.5V)
MOD and BIAS Voltage .....(V_{EE} + 1.0V) to +0.5V
MODN1 and MODN2 Voltage .....-0.5V to +0.5V
Operating Junction Temperature .....-55°C to +150°C
Storage Temperature Range .....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.9V to -5.5V ±6%, T_A = -40°C to +85°C. Typical values are at V_{EE} = -5.2V, V_{CC} = +3.3V, I_{BIAS} = 16.7mA, I_{MOD} = 83.3mA, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Voltage	V_{EE}		-5.5	-5.2	-4.9	V
Power-Supply Current	I_{EE}	Excluding bias and modulation current		106	140	mA
Single-Ended Input Resistance		Input to V_{TT}	40	50	60	Ω
Bias Current-Setting Range	I_{BIAS}	I_{BIAS} defined in Figure 3	1.0		40	mA
Bias Current-Setting Error		Bias current = 40mA, T_A = +25°C	-10		+10	%
		Bias current = 1mA, T_A = +25°C	-5		+5	
Bias Sensing Resistor	R_{BIAS}		6.7	7.5	8.3	Ω
Bias Current Temperature Stability		I_{BIAS} = 40mA (Note 2)	-480		+480	ppm/°C
		I_{BIAS} = 1mA		-200		
Bias Off-Current		BIASSET ≤ (V_{EE} + 0.4V)			0.05	mA
$\overline{MODEN}$ and $\overline{RTEN}$ Input High	V_{IH}		V_{EE} + 2.0			V
$\overline{MODEN}$ and $\overline{RTEN}$ Input Low	V_{IL}				V_{EE} + 0.8	V
Power-Supply Rejection Ratio	PSRR	f ≤ 10MHz, 100mVp-p (Note 8)		50		dB
SIGNAL INPUT FOR V_{TT} = 0						
Single-Ended Input (DC-Coupled)	V_{IS}	At high		0		V
		At low	-1.0		-0.15	
Single-Ended Input (AC-Coupled)	V_{IS}	At high	+0.075		+0.4	V
		At low	-0.4		-0.075	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = -4.9V to -5.5V ±6%, T_A = -40°C to +85°C. Typical values are at V_{EE} = -5.2V, V_{CC} = +3.3V, I_{BIAS} = 16.7mA, I_{MOD} = 83.3mA, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Input Swing (DC-Coupled)	V_{ID}		0.3		2.0	Vp-p
Differential Input Swing (AC-Coupled)	V_{ID}		0.3		1.6	Vp-p
SIGNAL INPUT FOR V_{TT} = -1.3V						
Input Common Mode	V_{ICM}			-1.3		V
Single-Ended Input	V_{IS}	At high	-1.225		-0.8	V
		At low	-1.8		-1.375	
Differential Input Swing	V_{ID}		0.3		2.0	Vp-p

AC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.9V to -5.5V ±6%, T_A = -40°C to +85°C. Typical values are at V_{EE} = -5.2V, V_{CC} = +3.3V, I_{BIAS} = 16.7mA, I_{MOD} = 83.3mA, T_A = +25°C, unless otherwise noted.) (Notes 1, 4, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Data Rates		NRZ (Note 2)		10.7		Gbps
Input Return Loss	RL_{IN}	f ≤ 15GHz (Notes 2, 6)		15		dB
Modulation Current-Setting Range	I_{MOD}	I_{MOD} defined in Figure 3 (Note 7)	20		100	mA
Modulation Current-Setting Error		T_A = +25°C	-10		+10	%
Modulation Sensing Resistor	R_{MOD}		2.7	3.0	3.3	Ω
Modulation Current Temperature Stability		I_{MOD} = 100mA (Note 2)	-550		+550	ppm/°C
		I_{MOD} = 20mA		-200		
Modulation Off-Current		MODSET ≤ (V_{EE} + 0.4V)			0.1	mA
Output Back Termination Resistor			63.8	75.0	86.3	Ω
Output Edge Speed	t_R, t_F	Z_L = 50Ω, 20% to 80% (Note 3)		34		ps
Setup/Hold-Time	t_{SU}, t_{HD}	Figure 2 (Notes 2, 3)		8	±25	ps
Pulse-Width Adjustment Range		Z_L = 50Ω, at 10Gbps (Notes 2, 3)		±60		ps
Pulse-Width Stability		PWC+ and PWC- open (Notes 2, 3)	-6		+6	ps
Pulse-Width Control Input Range		For PWC+ and PWC-	V_{EE}	V_{EE} + 1.0	V_{EE} + 2.0	V

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = -4.9V to -5.5V ±6%, T_A = -40°C to +85°C. Typical values are at V_{EE} = -5.2V, V_{CC} = +3.3V, I_{BIAS} = 16.7mA, I_{MOD} = 83.3mA, T_A = +25°C, unless otherwise noted.) (Notes 1, 4, 5)

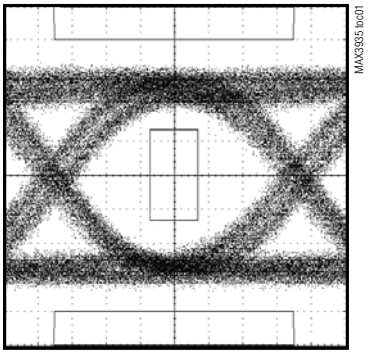
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Overshoot	δ	(Note 3)		1		%V
Driver Random Jitter		(Note 3)		0.75		ps_{RMS}
Driver Deterministic Jitter		(Note 5)		11		ps_{p-p}

Note 1: Specifications at -40°C are guaranteed by design and characterization.
Note 2: Guaranteed by design and characterization.
Note 3: Measured using a 10.7Gbps repeating 0000 0000 1111 1111 pattern.
Note 4: AC characterization performed using the circuit in Figure 1.
Note 5: Measured using a 10.7Gbps 2^{13} -1 PRBS with 80 0's + 80 1's input data pattern.
Note 6: For both data inputs DATA+, DATA- and clock inputs CLK+, CLK-.
Note 7: Load impedance is 50Ω in parallel with an internal 75Ω termination.
Note 8: PSRR = $20 \times \log_{10} (V_{NOISE\ (ON\ VCC)}/(\Delta I_{MOD} \times 30\Omega))$. Excludes the effect of the external op amp.

Typical Operating Characteristics

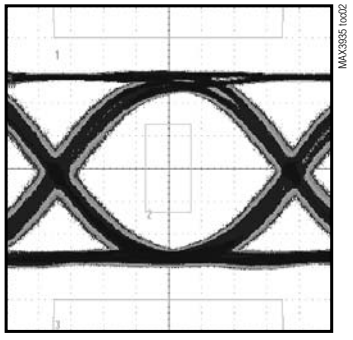
(T_A = +25°C, unless otherwise noted.)

OPTICAL EYE DIAGRAM (I_{MOD} = 100mA, 2^{13}-1 +80CID)



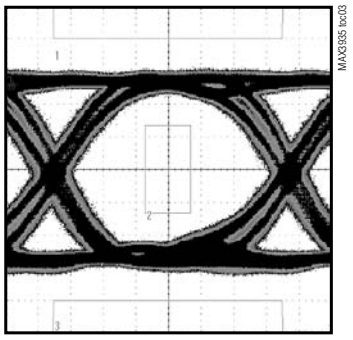
14ps/div

ELECTRICAL EYE DIAGRAM (I_{MOD} = 100mA, 2^{13} -1 +80CID)



13ps/div

ELECTRICAL EYE DIAGRAM (I_{MOD} = 20mA, 2^{13} -1 +80CID)

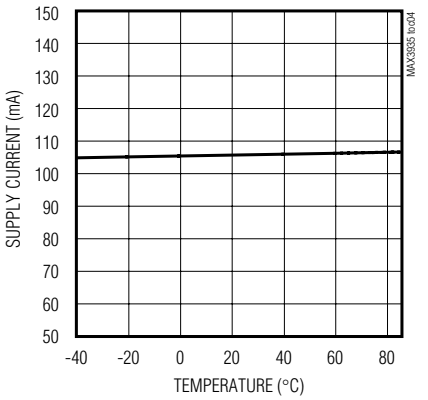


13ps/div

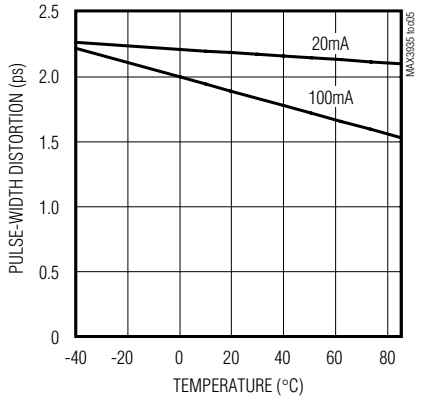
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

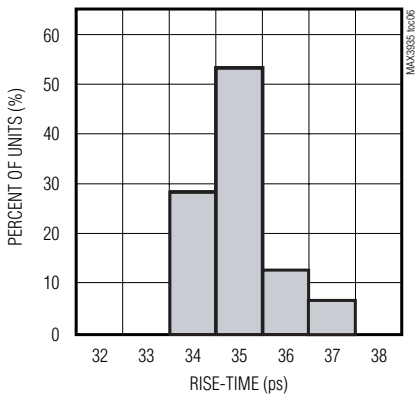
SUPPLY CURRENT (I_{EE}) vs. TEMPERATURE (EXCLUDES BIAS AND MODULATION CURRENTS)



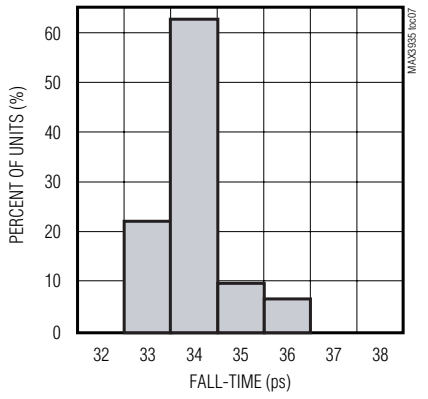
PULSE-WIDTH DISTORTION vs. TEMPERATURE



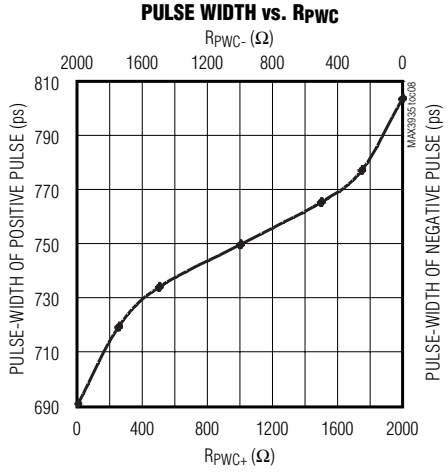
TYPICAL DISTRIBUTION OF RISE-TIME



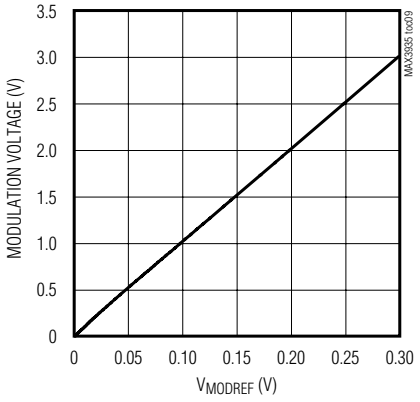
TYPICAL DISTRIBUTION OF FALL-TIME



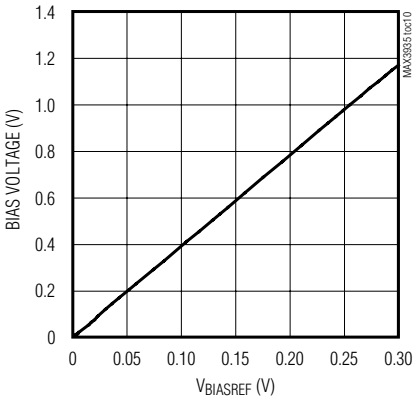
PULSE WIDTH vs. R_{PWC}



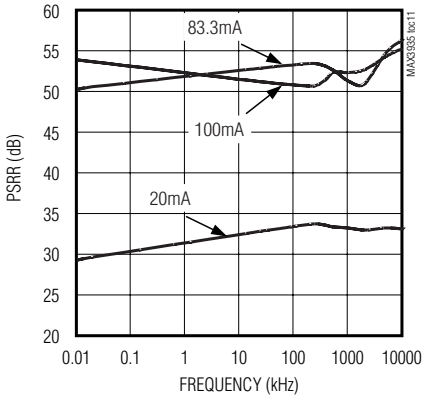
MODULATION VOLTAGE vs. V_{MODREF}



BIAS VOLTAGE (50Ω) LOAD vs. $V_{BIASREF}$



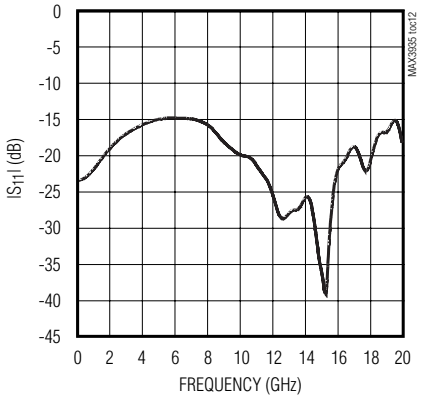
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



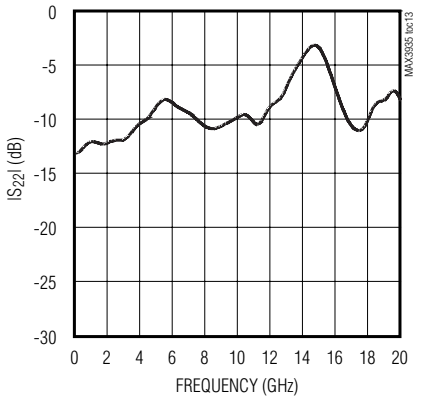
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

DIFFERENTIAL S_{11} vs. FREQUENCY



S_{22} vs. FREQUENCY WITH POWER OFF



Pin Description

PIN	NAME	FUNCTION
1, 4	V_{TT}	Termination Reference Voltage for Data Inputs
2	DATA+	Noninverting Data Input, with 50Ω On-Chip Termination
3	DATA-	Inverting Data Input, with 50Ω On-Chip Termination
5, 8	V_{TT}	Termination Voltage for Clock Inputs
6	CLK+	Noninverting Clock Input for Data Retiming, with 50Ω On-Chip Termination
7	CLK-	Inverting Clock Input for Data Retiming, with 50Ω On-Chip Termination
9	PWC+	Positive Input for Modulation Pulse-Width Adjustment. Connected to V_{EE} through R_{PWC}.
10	PWC-	Negative Input for Modulation Pulse-Width Adjustment. Connected to V_{EE} through R_{PWC}.
11, 18, 22, 30	GND	Ground
12, 13, 17, 23, 28, 29	V_{EE}	Negative Supply Voltage
14	MODMON	Modulation Current Monitor. (V_{MODMON} - V_{EE}) / 3Ω = I_{MOD}.
15	MODSET	Modulation Current Set. Connected to the output of an external op amp (see *Design Procedure*).
16, 24	N.C.	No Connection. Leave unconnected.
19, 21	MODN2, MODN1	Complementary Modulation Output with On-Chip Resistive Load. Connect to GND.
20	MOD	Modulation Output, DC-Coupled to EAM
25	BIAS	EAM Bias Output. Connect to the EAM via an inductor.

Pin Description (continued)

PIN	NAME	FUNCTION
26	BIASSET	Bias Current Set. Connected to the output of an external op amp (see *Design Procedure*).
27	BIASMON	Bias Current Monitor. ($V_{BIASMON}$ - V_{EE}) / 7.5Ω = I_{BIAS}.
31	$\overline{MODEN}$	TTL/CMOS Modulation Enable Input. Low for normal operation, high to put the EAM in the absorption (logic 0) state. Internal 100kΩ pullup to GND.
32	$\overline{RTEN}$	TTL/CMOS Data Retiming Input. Low for retimed data, high to bypass retiming latch. Internal 100kΩ pullup to GND.

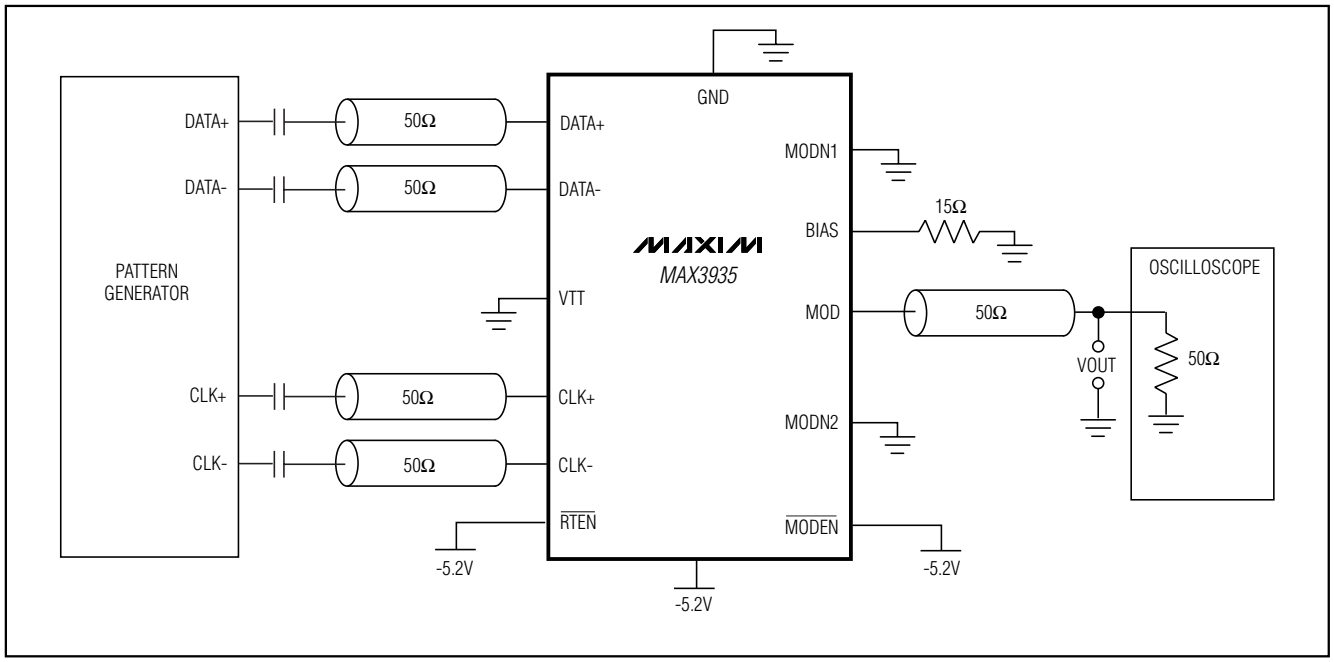


Figure 1. AC Characterization Circuit

Detailed Description

The MAX3935 EAM driver consists of a high-speed modulation driver and an EAM-biasing block (see Figure 3). The clock and data inputs to the modulation driver interface with ECL and CML logic levels. The modulation and bias outputs sink current to V_{EE} at -5.2V.

The modulation output stage is composed of a high-speed differential pair and a programmable current source with a maximum modulation current of 100mA. The rise- and fall-times are typically 34ps. The modulation current is designed to produce an EAM voltage up to 3.0Vp-p when driving a 50Ω module. The 3.0Vp-p results from 100mA through 50Ω in parallel with an internal 75Ω resistor (30Ω).

Any loading of the EAM module with capacitance will degrade the optical output performance. Since the BIAS output is connected to the EAM, minimize the parasitic capacitance associated with this pad by using an inductor (L) to isolate the BIAS pin from the EAM.

Clock/Data Input Logic Levels

The MAX3935 is directly compatible with 0V reference CML. Other logic interfaces are possible with AC-coupling capacitors. For 0V CML of AC-coupled logic, set V_{TT} to 0V. For other DC-coupled differential signals, set V_{TT} to the common-mode input voltage.

10.7Gbps EAM Driver

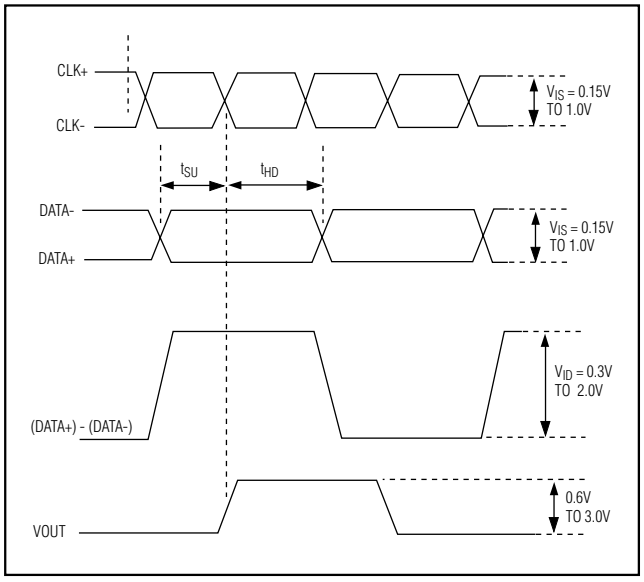


Figure 2. Required Input Signal, Setup/Hold-Time Definition and Output Polarity

Optional Input Data Retiming

To eliminate pattern-dependent jitter in the input data, a synchronous differential clock signal should be connected to the CLK+ and CLK- inputs, and the $\overline{RTEN}$ control input should be tied low. The input data is retimed on the rising edge of CLK+. If $\overline{RTEN}$ is tied high or left floating, the retiming function is disabled and the input data is directly connected to the output stage. Leave CLK+ and CLK- open when retiming is disabled.

Pulse-Width Control

The pulse-width control circuit can be used to minimize pulse-width distortion. The differential voltage between PWC+ and PWC- adjusts the pulse-width compensation. When PWC+ and PWC- are left open, the pulse-width control circuit is automatically disabled.

Modulation Output Enable

The MAX3935 incorporates a modulation current enable input. When $\overline{MODEN}$ is low, the modulation output (MOD) is enabled. When $\overline{MODEN}$ is high or floating, the output is disabled. In the disabled condition, the modulation output sinks current to keep the EAM module in the high-absorption state. The typical EAM enable time is 2ns, and the typical disable time is 5ns.

Current Monitors

The MAX3935 features a bias-current monitor output (BIASMON) and a modulation-current monitor output (MODMON). The voltage at BIASMON is equal to (I_{BIAS} × R_{BIAS}) + V_{EE} and the voltage at MODMON is equal to (I_{MOD} × R_{MOD}) + V_{EE}. I_{BIAS} and I_{MOD} are shown in Figure 3. The internal resistors R_{BIAS} and R_{MOD} are 7.5Ω and 3Ω, respectively (±10%). BIASMON and MODMON should be connected to the inverting input of an op amp to program the bias and modulation current (see *Design Procedure*).

Design Procedure

Programming the Modulation Voltage

The EAM modulation voltage results from I_{MOD} passing through the EAM impedance in parallel with the internal 75Ω-termination resistor.

$$V_{MOD} \approx I_{MOD} \times \frac{Z_{EAM} \times 75\Omega}{Z_{EAM} + 75\Omega}$$

To program the desired modulation current, connect the inverting input of an op amp (see *Typical Application Circuit*) to MODMON and connect the output to MODSET. Connect the positive op amp voltage supply to ground and the negative supply to V_{EE}. The modulation current is set by connecting a reference voltage V_{MODREF} to the noninverting input of the op amp. Refer to the Modulation Voltage vs. V_{MODREF} graph in the *Typical Operating Characteristics* to select the value of V_{MODREF} that corresponds to the required modulation current.

$$I_{MOD} = \frac{V_{MODREF}}{3\Omega}$$

Programming the Bias Voltage

The EAM bias voltage results from I_{BIAS} passing through the EAM impedance in parallel with the internal 75Ω-termination resistor.

$$V_{BIAS} \approx I_{BIAS} \times \frac{Z_{EAM} \times 75\Omega}{Z_{EAM} + 75\Omega}$$

To program the desired EAM bias current, connect the inverting input of an op amp (see *Typical Application Circuit*) to BIASMON and connect the output to BIASSET. Connect the positive op amp voltage supply to ground and the negative supply to V_{EE} . The EAM bias current is set by connecting a reference voltage $V_{BIASREF}$ to the noninverting input of the op amp. Refer to the Bias Voltage vs. $V_{BIASREF}$ graph in the *Typical Operating Characteristics* to select the value of V_{BIAS} that corresponds to the required EAM bias voltage.

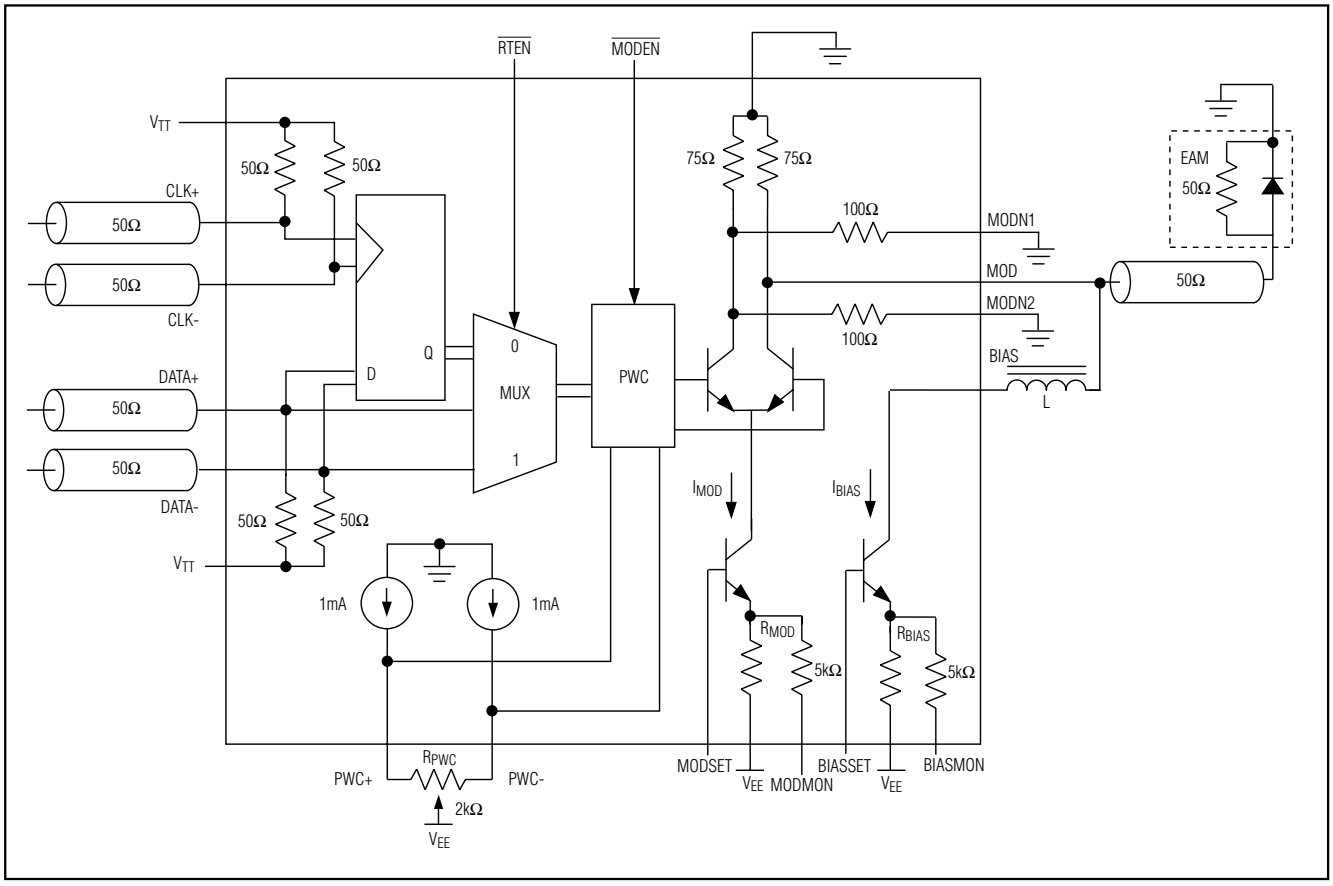


Figure 3. Functional Diagram

$$I_{BIAS} = \frac{V_{BIASREF}}{7.5\Omega}$$

To keep the bias and modulation currents in compliance, the following constraint on the total current must be made for 50Ω EAM modules:

$$|V_{EE}| - (I_{BIAS} + I_{MOD}) \times 30\Omega \geq 1.55V$$

External Op Amp Selection

External op amps are required for regulating the bias and modulation currents. The ability to operate from a single supply with input common-mode range extending to the negative supply rail is critical in the op amp selection. Low bias current and high PSRR are also important. Bias current to the inverting input passes through a 5kΩ resistor. This could add an error to the voltage produced by the modulation and bias current-sense resistors. The op amp gain bandwidth must be high enough to regulate at the power-supply ripple frequency on V_{EE}.

Pulse-Width Control Setup

Two methods of control are possible when pulse predistortion is desired to minimize distortion at the receiver. The pulse width may be set with a 2kΩ potentiometer (or equivalent fixed resistors) or by applying a voltage, with V_{EE} + 1V common mode, to the PWC pins may set it. Refer to Table 1 for the desired effect of the pulse width setting.

Table 1. Pulse-Width Control

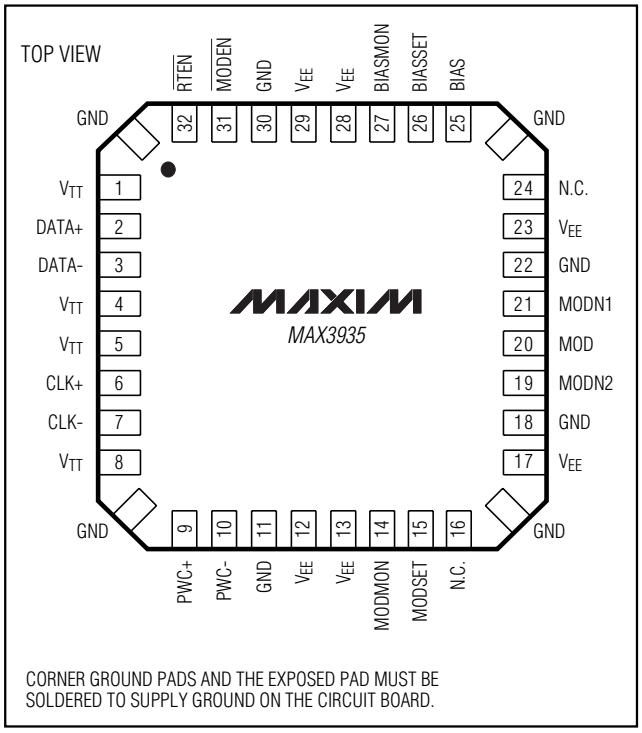
PULSE WIDTH	RP, RN for RP + RN = 2kΩ	V_{PWC+}, V_{PWC-} for $V_{CM} = V_{EE} + 1V$
100%	1kΩ or Open	$V_{PWC+} = V_{PWC-} = V_{EE} + 1V$
>100%	RP > RN	$V_{PWC+} > V_{PWC-}$
<100%	RP < RN	$V_{PWC+} < V_{PWC-}$

Applications Information

Layout Considerations

To minimize loss and crosstalk, keep the connections between the MAX3935 output and the EAM module as short as possible. Use good high-frequency layout techniques and multilayer boards with uninterrupted ground plane to minimize EMI and crosstalk. Circuit boards should be made using low-loss dielectrics. Use controlled-impedance lines for the clock and data inputs as well as the modulation output.

Pin Configuration



CORNER GROUND PADS AND THE EXPOSED PAD MUST BE SOLDERED TO SUPPLY GROUND ON THE CIRCUIT BOARD.

Input and Output Schematics

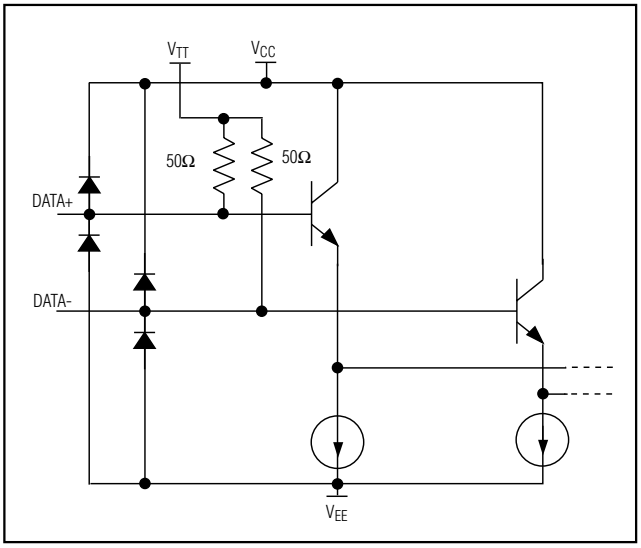
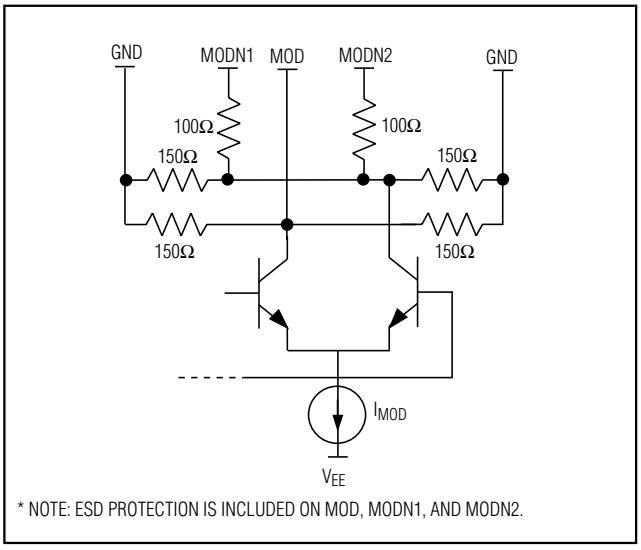


Figure 4. Equivalent Input Circuit



* NOTE: ESD PROTECTION IS INCLUDED ON MOD, MODN1, AND MODN2.

Figure 5. Equivalent Output Circuit

Chip Information

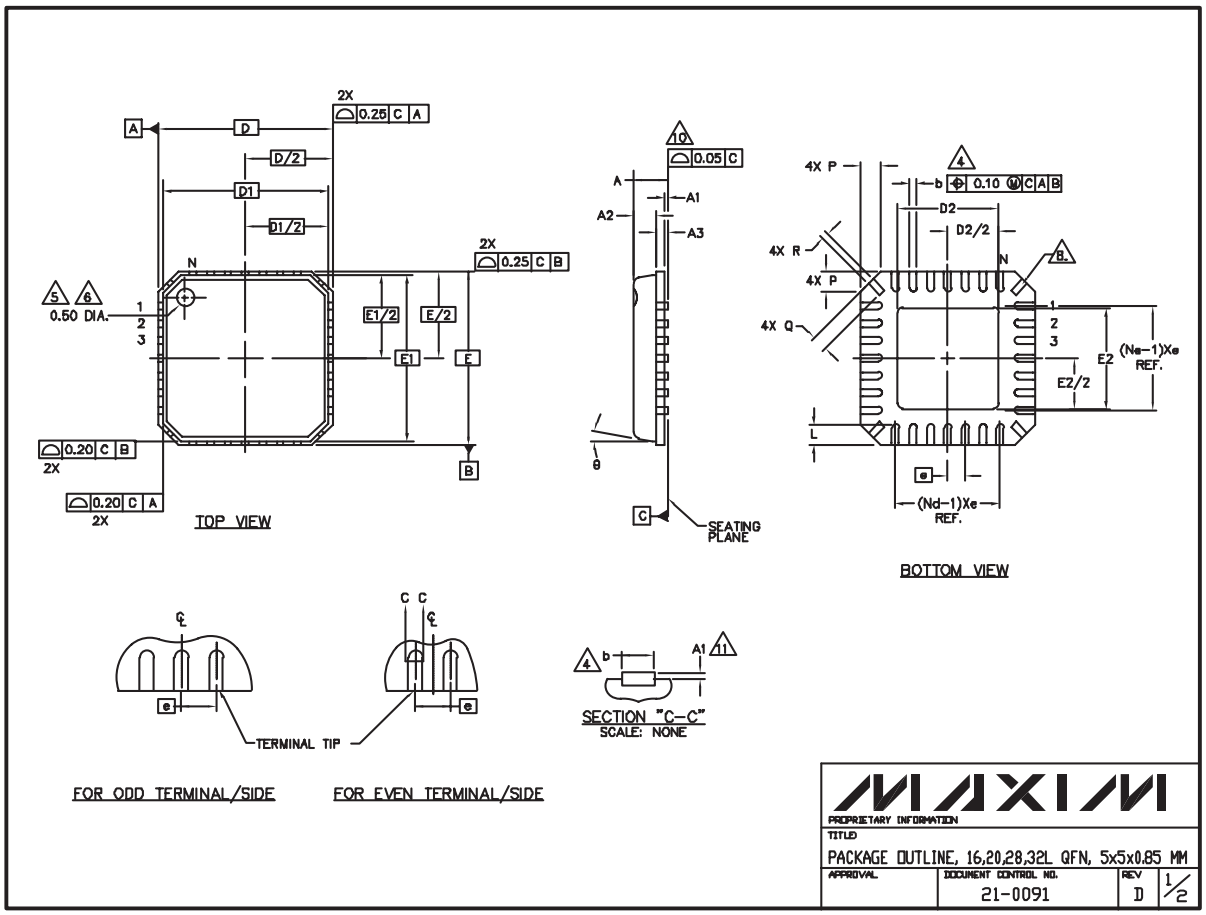
TRANSISTOR COUNT: 1535

SUBSTRATE: SOI

PROCESS: BIPOLAR SILICON GERMANIUM

Package Information

32L QFN, 5x5x0.85.EPS



Package Information (continued)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.05mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.
    EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.85	1.00	
A1	0.00	0.01	0.05	11
A2	–	0.65	0.80	
A3		0.20 REF.		
D		5.00 BSC		
D1		4.75 BSC		
E		5.00 BSC		
E1		4.75 BSC		
θ			12°	
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	

SYMBOL	PITCH VARIATION A			NOTE	SYMBOL	PITCH VARIATION B			NOTE	SYMBOL	PITCH VARIATION C			NOTE	SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.			MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
e	0.80 BSC				e	0.65 BSC				e	0.50 BSC				e	0.50 BSC			
N	16			3	N	20			3	N	28			3	N	32			3
Nd	4			3	Nd	5			3	Nd	7			3	Nd	8			3
Ne	4			3	Ne	5			3	Ne	7			3	Ne	8			3
L	0.50	0.60	0.75		L	0.50	0.60	0.75		L	0.50	0.60	0.75		L	0.30	0.40	0.55	
b	0.28	0.33	0.40	4	b	0.23	0.28	0.35	4	b	0.18	0.23	0.30	4	b	0.18	0.23	0.30	4
Q	0.30	0.40	0.65		Q	0.30	0.40	0.65		Q	0.30	0.40	0.65		Q	0.00	0.20	0.45	
D2	SEE EXPOSED PAD VARIATION:B				D2	SEE EXPOSED PAD VARIATION:B				D2	SEE EXPOSED PAD VARIATION:A,B				D2	SEE EXPOSED PAD VARIATION:A			
E2	SEE EXPOSED PAD VARIATION:B				E2	SEE EXPOSED PAD VARIATION:B				E2	SEE EXPOSED PAD VARIATION:A,B				E2	SEE EXPOSED PAD VARIATION:A			

SYMBOLS		D2			E2			NOTE
		MIN	NOM	MAX	MIN	NOM	MAX	
EXPOSED PAD VARIATIONS	A	2.95	3.10	3.25	2.95	3.10	3.25	
	B	2.55	2.70	2.85	2.55	2.70	2.85	

EXAMPLE: WE CAN CALL VARIATION "BB" FOR 20 TERMINAL QFN WITH 2.70mm X 2.70mm NOMINAL EXPOSED PAD DIMENSION. THE FORMER ONE IN VARIATION IS FOR PITCH VARIATION AND THE LETTER ONE IS FOR EXPOSED PAD VARIATION.

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.85 MM

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0091	D	2/2